REMARKS

Claim 40 has been amended. Claims 1-67 remain pending in the application. Reconsideration is respectfully requested in light of the following remarks.

Section 112, Second Paragraph, Rejection:

The Office Action rejected claims 40-61 under 35 U.S.C. § 112, second paragraph as indefinite. Claim 40 has been amended for clarity. Applicants assert that claim 40 is definite and respectfully request withdrawal of the rejection.

Section 103(a) Rejection:

The Office Action rejected claims 1-9, 19, 21-27, 29-48, 52-64 and 66-67 under 35 U.S.C. § 103(a) as being unpatentable over McAuliffe et al. (U.S. Patent 6,367,047) (hereinafter "McAuliffe") in view of Bruckert et al. (U.S. Patent 5,153,881) (hereinafter "Bruckert"). Applicants respectfully traverse these rejections.

In regard to claim 1, the cited art does not teach or suggest a data integrity device that is configured to be enabled and disabled, wherein if the data integrity device is disabled, the host computer system and the storage array provide a first level of error protection for the data, and if the data integrity device is enabled, at least one processor of the data integrity device is configured to perform a first data integrity operation on the data in order to provide a second level of error protection for the data in addition to the first level of error protection provided by the host computer system and the storage array. Instead, McAuliffe discloses a multi-level error correction technique for maintaining data integrity in a data recording/recovery device (Abstract). McAuliffe does not teach that its error detection and correction can be enabled and disabled. The validity/invalidity indications cited by the Examiner in Column 56, lines 65 through Column 7, line 25, are used to identify which portions of a data buffer currently contain data, and which portions are not used. The invalidity or

non-use of portions of a segment has nothing to do with enabling or disabling the error correction/detection. Furthermore, the multi-level error correction taught by McAuliffe pertains to performing error correction "at both the packet level and at the segment level." McAuliffe -- col. 2, lines 40-44. McAuliffe's multi-level error correction does not teach or suggest a first level of error protection provided by the host computer system and the storage array if the data integrity device is disabled and, if the data integrity device is enabled, a second level of error protection provided by the data integrity device in addition to the first level of error protection provided by the host computer system and the storage array. The multi-level error correction in McAuliffe does not provide a first level of protection if a data integrity device is disabled and a second level in addition to the first level if the data integrity device is enabled. Nor does McAuliffe teach or suggest one level of protection provided by the host computer system and the storage array and a second level provided by a data integrity device.

Nor is Bruckert, when considered either alone or in combination with McAuliffe, in any way suggestive of the above noted features recited in claim 1. Bruckert discloses a method and apparatus for processing errors in a fault- tolerant computing system which has dual processors operating in synchronism (Column 1, lines 1-5). An attempt is made to locate the source of an error in hardware and disable a processor if it is faulty prior to entering software error handling routines (Column 1, lines 50-53). Although Bruckert discloses disabling a faulty processor or device, Bruckert teaches nothing of disabling a data integrity device – in fact, the disabling of a faulty processor or device occurs only when data integrity operations detect the fault (e.g., see Column 28, lines 50-61). Thus, to maintain fault tolerance, Bruckert requires that its data integrity operation remain active at all times. Therefore, Bruckert actually teaches away from disabling a data integrity device. Moreover, Bruckert teaches nothing of a first level of error protection provided by a host computer system and a storage array if a data integrity device is disabled and, if the data integrity device is enabled, a second level of error protection provided by the data integrity device in addition to the first level of error protection provided by the host computer system and the storage array.

Independent claim 39 of the present application recites a data integrity device comprising a plurality of processors configured to be individually enabled or disabled, wherein each processor is configured to perform a data integrity operation on data being transferred between a host computer system and a storage array. McAuliffe and Bruckert do not teach a data integrity device with multiple processors, where each processor may be individually enabled or disabled. Applicants also note that claim 11 recites essentially the same limitation and the Examiner indicated that claim 11 would be allowable. Thus, it is unclear why the Examiner did not also find claim 39 allowable.

In addition, claim 39 recites that the number of processors enabled in the data integrity device corresponds to a user-selected level of error protection. McAuliffe and Bruckert do not teach or suggest this feature.

In regard to independent claim 40, McAuliffe and Bruckert does not teach or suggest a plurality of processors in a data integrity device, each performing a data integrity operation on data transferred between a host computer system and a storage array. Applicants can find no teaching or suggestion in either McAuliffe or Bruckert of performing data integrity operations at each processor of a plurality of processors on data being transferred to a storage array.

Further in regard to claim 40, McAuliffe and Bruckert does not teach or suggest a comparison of the data integrity operation results from each of the plurality of processors to provide an indication that the data transferred between a host computer system and a storage array is erroneous. Note that the fault tolerant operation of Bruckert applies to the operation of the processors, not the integrity of data transferred between a host computer system and a storage array.

In regard to claim 62, McAuliffe and Bruckert do not teach or suggest performing a first data transfer between a host computer system and a storage array, wherein a data integrity device is disabled during said performing, and subsequent to enabling the data integrity device, the data integrity device performing a data integrity operation on data

transferred in a second data transfer. As discussed above in regard to claim 1, neither McAuliffe nor Bruckert teaches a data transfer between a host computer system and a storage array with a data integrity device disabled, and another data transfer between the host computer system and the storage array with the data integrity device enabled. Similarly, in regard to claim 66, McAuliffe and Bruckert do not teach or suggest that one or more processors of a data integrity device are configured to be enabled and disabled.

In regard to claim 67, McAuliffe and Bruckert do not teach or suggest a means for performing a data integrity operation, wherein the means is responsive to various settings, and wherein one of the settings disables the means, wherein if the means for performing the data integrity operation are disabled, host computing means and storage means provide a first level of error protection for data, and if the means for performing the data integrity operation are enabled, a second level of error protection is provided for the data in addition to the first level. As discussed above in regard to claim 1, McAuliffe and Bruckert teach nothing of a first level of error protection provided by a host computing means system and a storage means if a data integrity means is disabled and, if the data integrity means is enabled, a second level of error protection provided by the data integrity means in addition to the first level of error protection provided by the host computing means and the storage means.

For at least the reasons cited above, Applicants respectfully submit that the rejection of independent claims 1, 39, 40, 62, 66 and 67 is clearly not supported by the teachings of McAuliffe and Bruckert, and removal of the rejection is respectfully requested.

Applicants also assert that the rejection of numerous ones of the dependent claims is further unsupported by the teachings of the cited art. However, since the rejection of the independent claims has been shown to be improper, a further discussion of the rejection of the dependent claims is not necessary at this time.

Allowable Subject Matter

Claims 10-18, 20-28, 49-51 and 65 were objected to as being dependent upon a rejected base claim but otherwise allowable if rewritten in independent form. In light of the above remarks, Applicants assert that claims 10-18, 20-28, 49-51 and 65 are allowable as depending from patentably distinct base claims. Applicants therefore respectfully request allowance of claims 10-18, 20-28, 49-51 and 65 as currently pending.

CONCLUSION

Applicants submit the application is in condition for allowance, and notice to that effect is respectfully requested.

If any extension of time (under 37 C.F.R. § 1.136) is necessary to prevent the above referenced application from becoming abandoned, Applicants hereby petition for such extension. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5681-04700/RCK.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

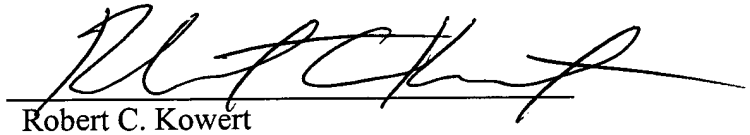
☐ Petition for Extension of Time

☐ Notice of Change of Address

☐ Fee Authorization Form authorizing a deposit account debit in the amount of $ for fees ( ).

☐ Other:

Respectfully submitted,



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